

REMARKS

The present application was filed on November 21, 2003 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1 and 8 under 35 U.S.C. §102(e) as being anticipated by Horie et al. (United States Patent Number 6,054,887); rejected claims 3, 4, 7, 10, 11 and 13 under 35 U.S.C. §103(a) as being unpatentable over Horie et al. in view of Beauducel et al. (United States Patent Number 4,352,070); rejected claims 6 and 12 under 35 U.S.C. §103(a) as being unpatentable over Horie et al. in view of Mills et al. (United States Patent Number 5,172,117); rejected claims 2, 5, 9, 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Horie et al. in view of Sandusky et al. (United States Patent Number 5,825,571); rejected claims 16, 17, 18 and 20 under 35 U.S.C. §103(a) as being unpatentable over Horie et al. and Sandusky et al., and further in view of Beauducel et al.; and rejected claim 19 under 35 U.S.C. §103(a) as being unpatentable over Horie et al. and Sandusky et al., and further in view of Mills et al.

Independent Claims 1, 8 and 14

Independent claims 1 and 8 were rejected under 35 U.S.C. §102(e) as being anticipated by Horie et al. In particular, the Examiner asserts that Horie et al. disclose a sample and hold circuit having an input and an output. Among other features, the Examiner asserts that Horie et al. also disclose at least one output switch for selectively connecting said at least one capacitive element to said output (citing Switches 22 and 24 of FIG. 10 as the output switches to the output “which is the DAC element, as disclosed in Col. 6, lines 21-33”).

First, Applicants note that Horie et al. is **not** a sample and hold circuit, as required by each independent claim. As set forth in the Brief Description of Figures, “FIG. 10 is a diagram of an *offset voltage correction circuit* and an operational amplifier.” (Col. 4 lines, 58-60). The fourth embodiment of FIG. 10 is said to be similar to the first embodiment of FIG. 1, except for a number of design changes that are not pertinent here, *see* col. 18, line 65, through col. 19, line 4, (FIG. 10 includes a resistor 300 that replaces the control circuit 19 of FIG. 1 and includes a microcomputer 301 that replaces the microcomputer 18 of FIG. 1). Thus, the description of the pertinent portions of FIG. 1 apply to FIG. 10 as well.

In addition, the input of the circuit shown in FIG. 10 is node **30** (see, col. 5, lines 10-21), and the output is node **3** (see., e.g., col. 5, lines 11-12). As previously indicated, the Examiner asserts

on page 2 that the output of the purported sample and hold circuit is the DAC element, as disclosed in Col. 6, lines 21-33". As read by Applicants, this passage only asserts that the DAC *has* an output (that is connected via switches 22, 24 to the gate of the transistors 17, 16) and not that it *is* the output of the overall circuit. In fact, the DAC 20 is an *input* to the operational amplifier 1 that is used to adjust the offset of the amplifier 1.

The Switches 22 and 24 of FIGS. 1 and 10 do **not** selectively connect the capacitive element 14 to the *output* 3 of the purported sample and hold circuit. Applicants can find no switch in Horie et al. that selectively connects the capacitive element 14 to the output 3.

Thus, Horie et al. do not disclose or suggest "at least one output switch for selectively connecting said at least one capacitive element to said output," as required by each independent claim. In addition, as recognized by the Examiner, Horie et al. do not disclose or suggest "a magneto-resistive read head," as further required by independent claim 14.

Applicants can also find no teaching of "at least one output switch for selectively connecting said at least one capacitive element to said output," in any of the additional cited references (Beauducel et al., Mills et al. or Sandusky et al.) and such a teaching in these additional cited references has not been asserted by the Examiner.

#### Dependent Claims 2-7, 9-13 and 15-20

Dependent claims 2-7, 9-13, and 15-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Horie et al. in view of one or more of Beauducel et al., Mills et al. and Sandusky et al. Claims 2-7, 9-13, and 15-20 are dependent on claims 1, 8, and 14, respectively, and are therefore patentably distinguished over Horie et al., Beauducel et al., Mills et al. and Sandusky et al., alone or in combination, because of their dependency from independent claims 1, 8, and 14 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

For example, claims 3, 10 and 16 require that at least one of the input and output switches has a leakage effect represented by a resistor in *parallel* with the input or output switch and a voltage drop across the resistor is limited to the offset voltage. The Examiner asserts that FIG. 4 of Beauducel et al. teaches a resistor, R<sub>1</sub>, placed in parallel. Applicants note, however, that resistor, R<sub>1</sub>, is in *series* with the current through switch I<sub>1</sub>. If the switch I<sub>1</sub> is in an open position, there is no current from the amplifier A<sub>1</sub> through the resistor R<sub>1</sub>.

All of the pending claims, i.e., claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully,



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